AMENDMENTS TO THE CLAIMS:

1. (Currently amended) An electronic camera in which an analog signal output from an image pickup device is analog-to-digital-converted (AD-converted) ~~AD-converted~~ and digital processing is performed on the AD-converted signal on the basis of a basic operating clock, said camera comprising:

a clock change device for ~~of~~ changing the frequency of the basic operating clock; and

a control device for ~~of~~ controlling the clock change device such ~~so~~ that the frequency of the basic operating clock is reduced at the time of AD conversion of a still image output from the image pickup device.

2. (Currently amended) The electronic camera according to claim 1, further comprising:

a photometry device for ~~of~~ measuring the brightness of a subject,

wherein said control device controls the clock change device such ~~so~~ that the frequency of the basic operating clock is reduced when it is determined that the brightness of the subject measured by said photometry device is lower than a predetermined brightness.

3. (Currently amended) The electronic camera according to claim 1, further comprising:

a photography mode selecting device for ~~of~~ selecting a desired photography mode from a plurality of photography modes,

wherein said control device controls the clock change device such ~~so~~ that the frequency of the basic operating clock is reduced only when a particular one of the photography modes is selected by said photography mode selecting device.

4. (Currently amended) The electronic camera according to claim 1, further comprising:

an International Standards Organization (ISO) ~~ISO~~ speed setting device for ~~of~~ setting an ISO speed,

wherein said control device controls the clock change device such ~~so~~ that the frequency of

the basic operating clock is reduced when the ISO speed set by said ISO speed setting device is equal to or higher than a predetermined value.

5. (Currently amended) The electronic camera according to claim 1, further comprising:

first and second line memories in which the AD-converted digital signal is alternately stored in a predetermined data amount, and a random access memory (RAM) ~~RAM~~ for temporarily storing the digital signal at least for one frame of a still image,

wherein, when capture of the digital signal in said first line memory is completed, the captured digital signal is direct memory access-transferred (DMA-transferred) ~~DMA-transferred~~ to said RAM on the basis of the basic operating clock, and

wherein, when capture of the digital signal in said second line memory is completed, the captured digital signal is DMA-transferred to said RAM on the basis of the basic operating clock signal.

6. (New) The electronic camera according to claim 1, further comprising:

an analog front end (AFE) which receives said analog signal output from an image pickup device, and comprises an analog-to-digital converter (A/D converter) which outputs said AD-converted signal.

7. (New) The electronic camera according to claim 6, further comprising:

a charge coupled device (CCD) image sensor which supplies said analog signal to said AFE; and

a clock generation circuit which supplies an AD clock signal to said A/D converter and said CCD image sensor.

8. (New) The electronic camera according to claim 7, wherein said analog front end further comprises:

a correlation double sampling (CDS) circuit which receives said analog signal, and

performs correlation double sampling on said analog signal;

a gain control amplifier (GCA) which controls a gain of a signal output from said CDS circuit, said A/D converter receiving said gain-controlled signal.

9. (New) The electronic camera according to claim 8, wherein said control device comprises a signal processor including plural line memories which alternately capture said AD-converted signal output from said AFE.

10. (New) The electronic camera according to claim 9, wherein said clock generation circuit supplies said basic operating clock to said signal processor which processes said AD-converted signal based on said basic operating clock.

11. (New) The electronic camera according to claim 9, wherein said clock generation circuit comprises a frequency divider for dividing a frequency of said basic operating clock.

12. (New) The electronic camera according to claim 9, wherein said clock change device comprises a clock change switch of said clock generation circuit,

wherein said signal processor supplies a clock change control signal to said clock change switch for causing a lever of said clock change switch to connect to a contact for supplying said basic operating clock to said frequency divider.

13. (New) The electronic camera according to claim 9, wherein said signal processor controls said frequency of said basic operating clock.

14. (New) The electronic camera according to claim 9, wherein said signal processor performs digital processing on the basis of said basic operating clock signal supplied from the clock signal generation circuit.

15. (New) The electronic camera according to claim 9, further comprising:

a random access memory (RAM) coupled to said signal processor, said plural line memories serving as a queue for a digital signal waiting to be direct memory access-transferred (DMA-transferred) to said RAM.

16. (New) The electronic camera according to claim 1, wherein said control device controls the clock change device such that the frequency of the basic operating clock is not reduced at a time which is other than the time of AD conversion of said still image.

17. (New) A signal processing circuit for an electronic camera including an image pickup device, said circuit comprising:

a clock change device for changing a frequency of a basic operating clock; and

a control device for controlling the clock change device such that the frequency of the basic operating clock is reduced at a time of AD conversion of a still image output from said image pickup device.

18. (New) A method of processing an image data signal in an electronic camera including an image pickup device, comprising:

changing a frequency of a basic operating clock; and

controlling the clock change device such that the frequency of the basic operating clock is reduced at a time of AD conversion of a still image output from said image pickup device.